**Lab 6**

**Implementation of a 8 bit Ring Counter**



**Spring 2025**

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Registration No: **22pwsce2149**

Class Section: **A**

“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”



Student Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_

Submitted to:

**Engr. Faheem Jan**

Month Day, Year (23 03, 2025)

Department of Computer Systems Engineering

University of Engineering and Technology, Peshawar

**Objective:**

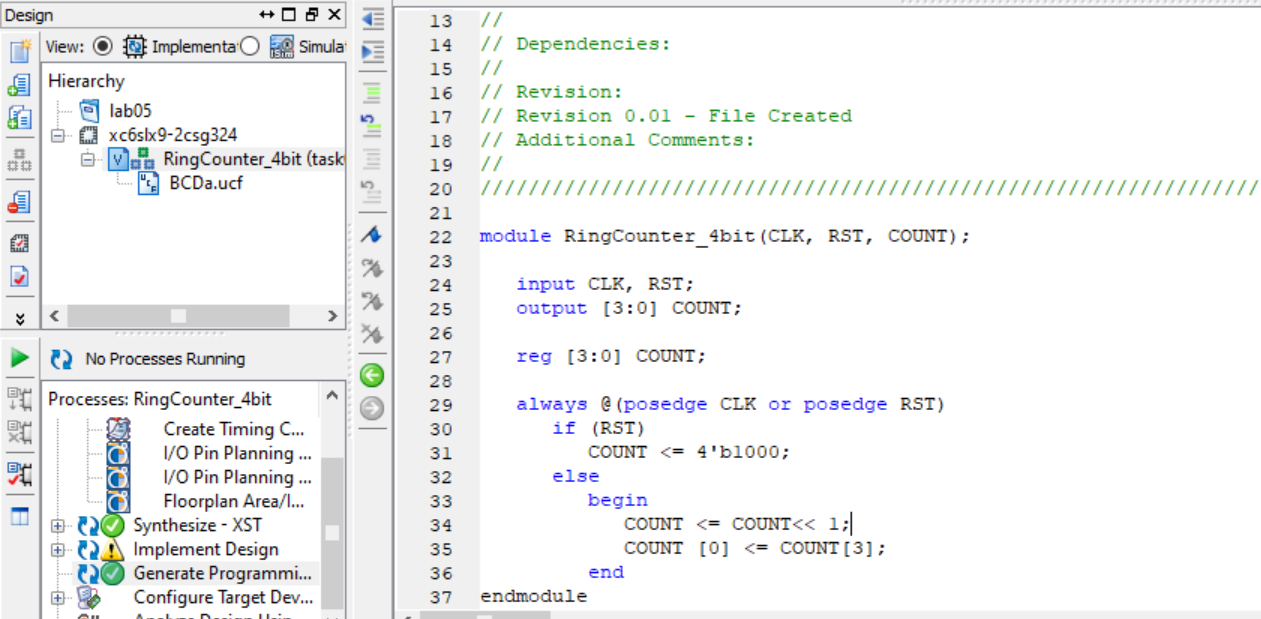
* To become familiarized with behavior level modeling
* To be able to implement sequential circuits using Verilog
* To Implement an 8 Bit Ring Counter on Spartan 6 FPGA starter kit.

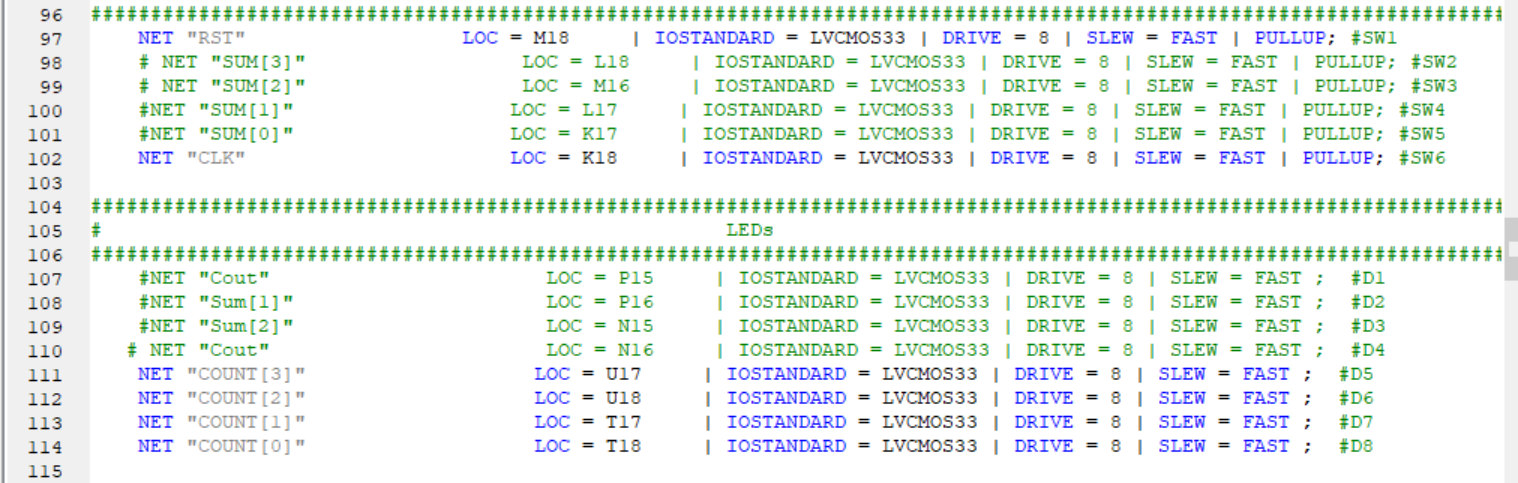
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**Lab Task:**

1-Implement 4 bit Ring Counter

**CODE:**

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**UCF file:  
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**OUTPUT:**

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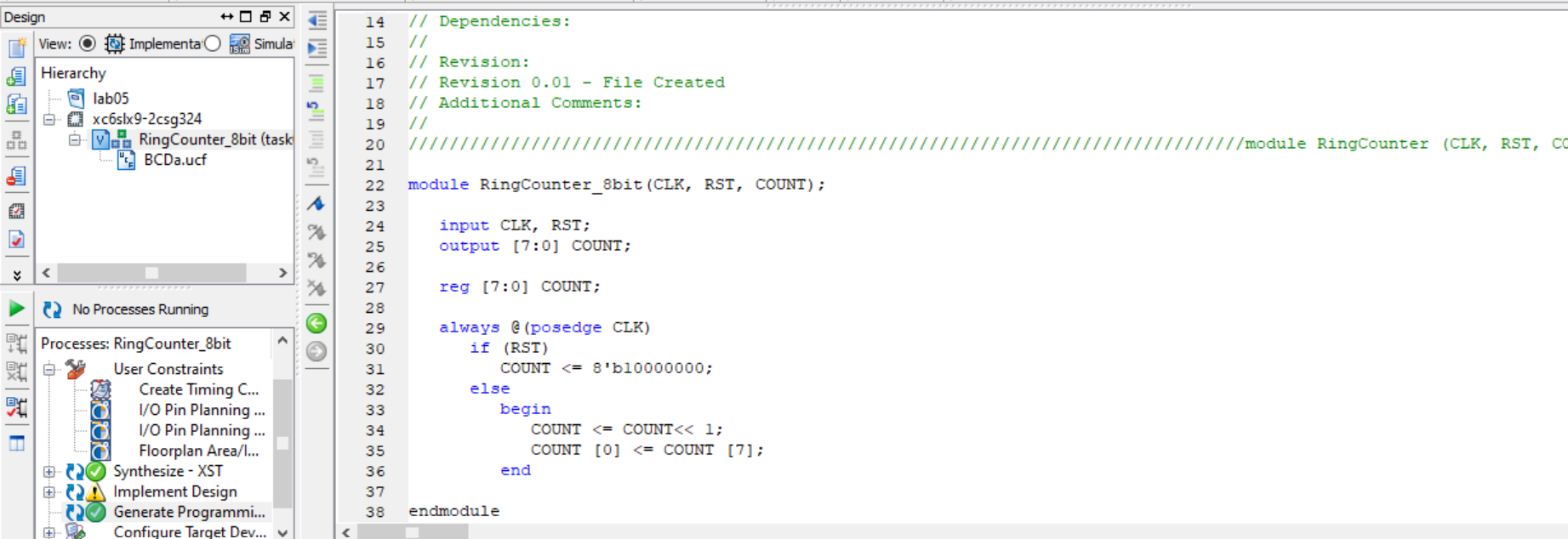
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**Conclusion:**

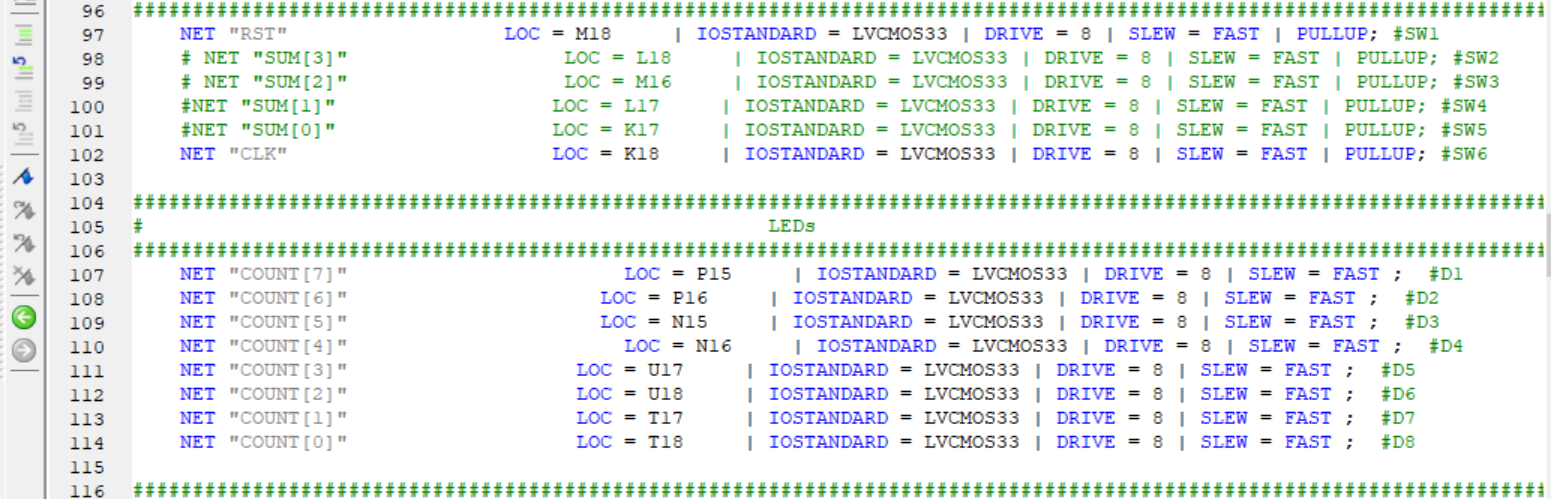
This **4-bit Ring Counter** shifts a single '1' through its four-bit register on each clock pulse. When **reset (RST) is high**, it initializes to 1000. On every **clock (CLK) pulse**, the bits shift left, and the leftmost bit wraps around to the rightmost position, creating a continuous rotating pattern. It is commonly used in **state machines** and **cyclic counting applications** in digital systems.

**TASK 02:**

Implement 8-bit Ring Counter   
**CODE:**



Ucf file:



**OUTPUT:**

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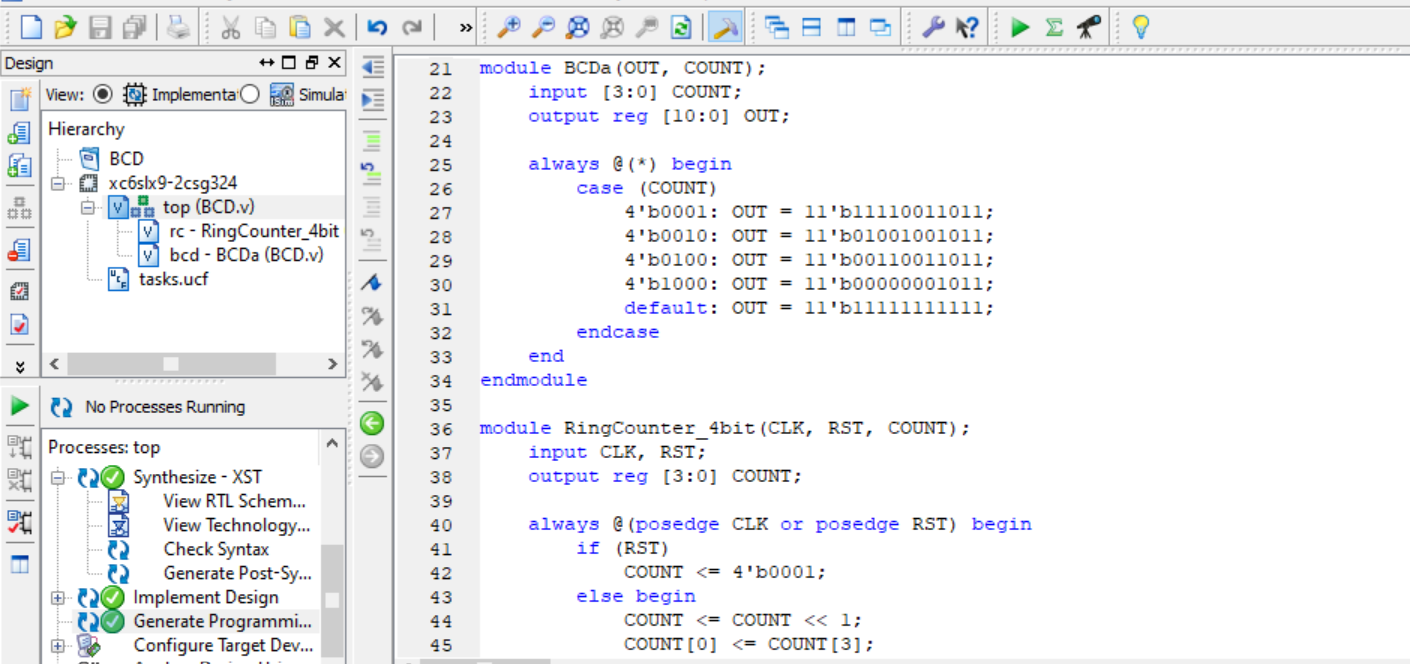
**Conclusion:**

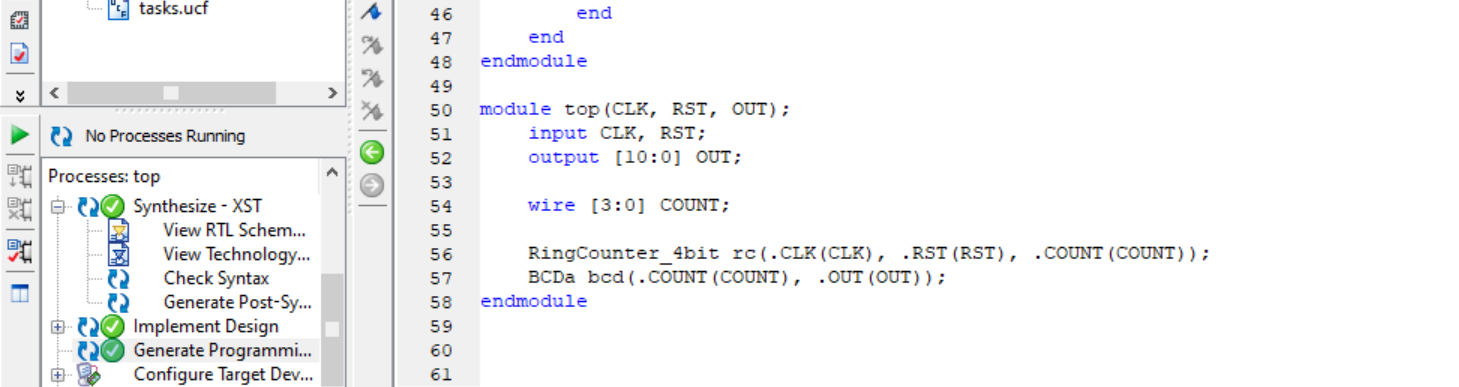
This 8-bit Ring Counter continuously shifts a single '1' through its 8-bit register on each clock cycle. When reset (RST) is high, it initializes to 10000000. On every clock (CLK) pulse, the bits shift left, and the leftmost bit wraps around to the rightmost position, creating a cyclic shifting pattern. This type of counter is useful in sequential circuits, state machines, and LED chasers.

**TASK 03:**

For 4 bit Ring counter display the count in the seven segment display.

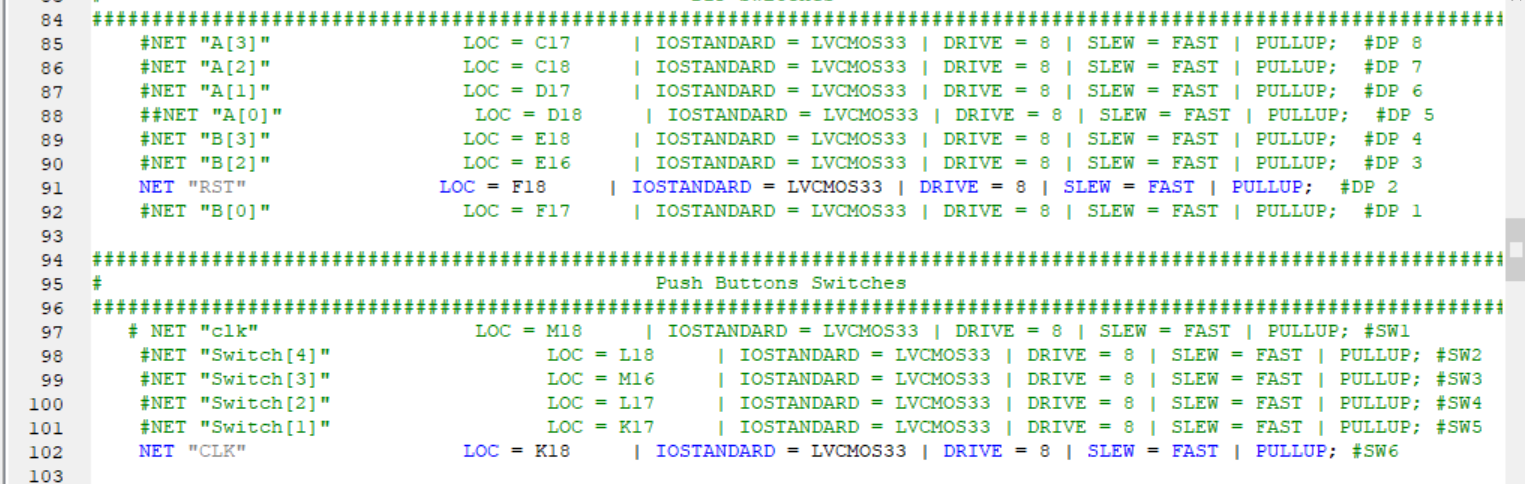
**CODE:**

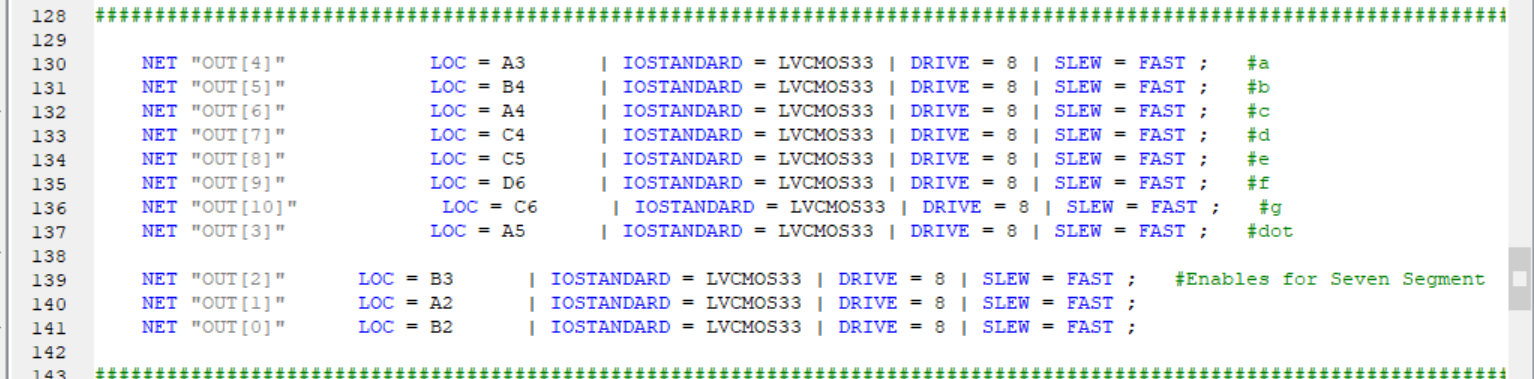
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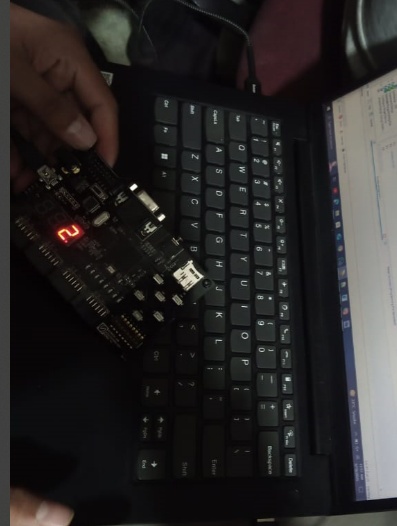
**UCF file:**

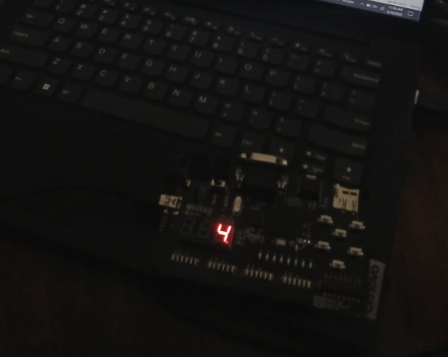
**Output:**

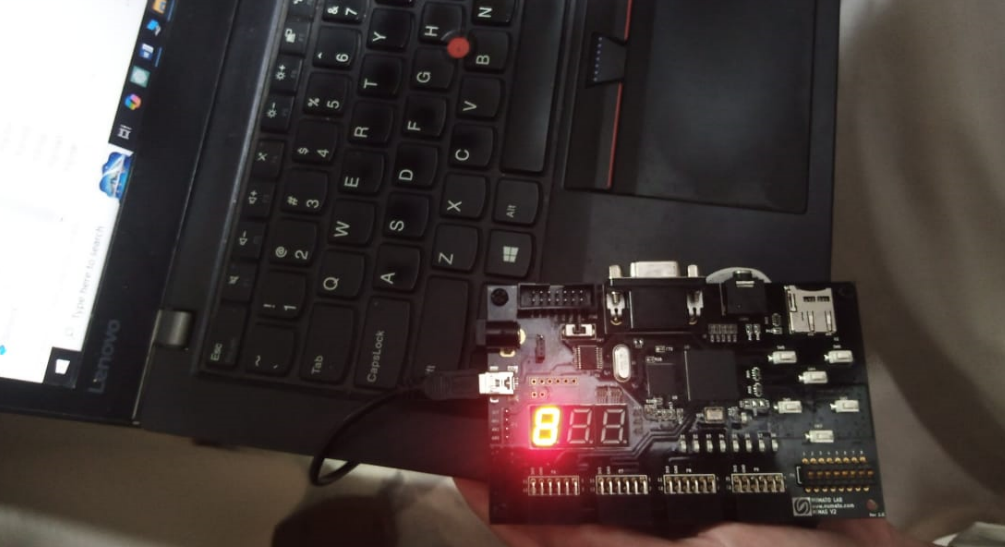
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**Output:**

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**Conclusion:**

This Verilog code implements a 4-bit Ring Counter and a BCD to 7-segmentdisplay decoder, then connects them in a top module.

1. **Ring Counter Module**
   * It cycles a single '1' through four positions.
   * On reset (RST), it starts at 0001.
   * On each clock (CLK) pulse, the bits shift left, and the last bit moves to the first position.
2. **BCD Decoder (BCDa) Module**
   * It converts a 4-bit binary count into an 11-bit output for display.
   * Specific BCD values (0001, 0010, 0100, 1000) map to predefined outputs.
3. **Top Module**
   * It connects the Ring Counter to the BCD Decoder.
   * The counter generates a sequence, and the decoder outputs the corresponding display value.

This setup is useful for sequential circuits, display systems, and LED animations.